Script generated by TTT

Title: Petter: Programmiersprachen (15.10.2014)

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Out-of-Order Execution

performance problem: writes always stall

Thread A

```
a = 1;      // A.1
b = 1;      // A.2
```

Thread B

```
while (b == 0) {};   // B.1
assert(a == 1);      // B.2
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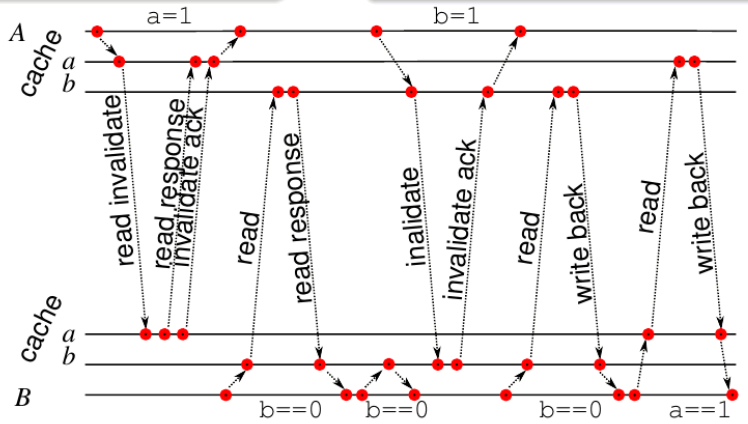


Summary

Sequential consistency:

- a characterization of well-behaved programs
- a model for different speed of execution
- for fixed paths through the threads *and* a total order between accesses to the same variable: executions can be illustrated by happened-before diagram with one process per variable
- MESI cache coherence protocol ensures SC for processors with caches

Disproving Sequential Consistency

Given a result of a program with n threads on a SC system,

1. with operations $p_0^1, p_1^1, \ldots$ and $p_0^2, p_1^2, \ldots$ and $\ldots p_0^n, p_1^n, \ldots$
2. there exists a total order $\exists C \,.\, C(p_i^j) < C(p_k^l)$ for all $i, j, k, l \ldots$ where $j = l$ implies $i < k$,
3. such that this execution has the same result.

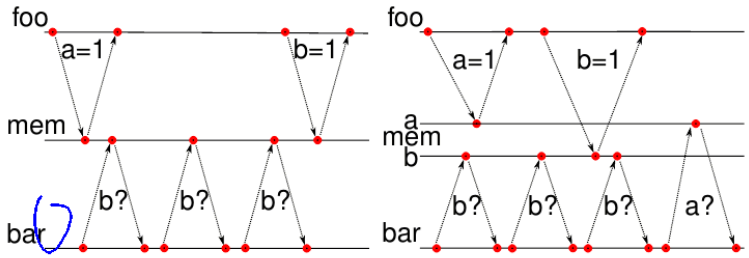
Idea for showing that a system is *not* sequentially consistent:

- pick a result obtained from a program run on a SC system
- pick an execution 1 and a total ordering of all operations 2
- add extra processes to model other system components
- the original order 2 becomes a partial order $\rightarrow$
- show that total orderings C' exist for $\rightarrow$ for which the result differ

Weakening the Model

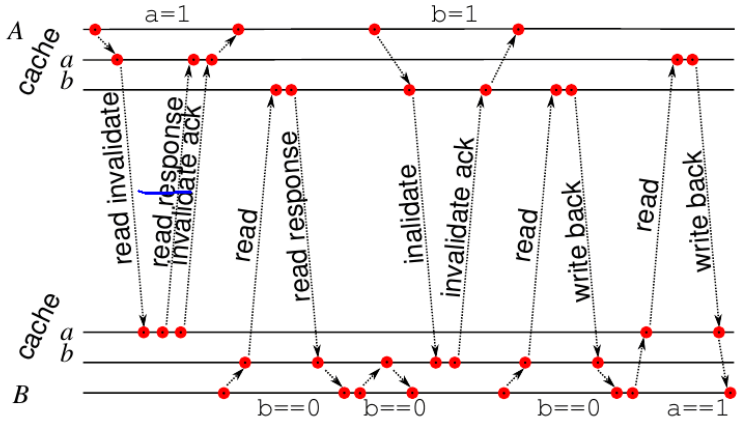
There is no observable change if calculations on different memory locations can happen in parallel.

- idea: model each memory location as a different process



MESI Example: Happened Before Model

Idea: each cache line one process, A caches b=0 as E, B caches a=0 as E



Observations:

- each memory access must complete before executing next instruction
  ⇝ add edge
- second execution of test `b==0` stays within cache ⇝ no traffic

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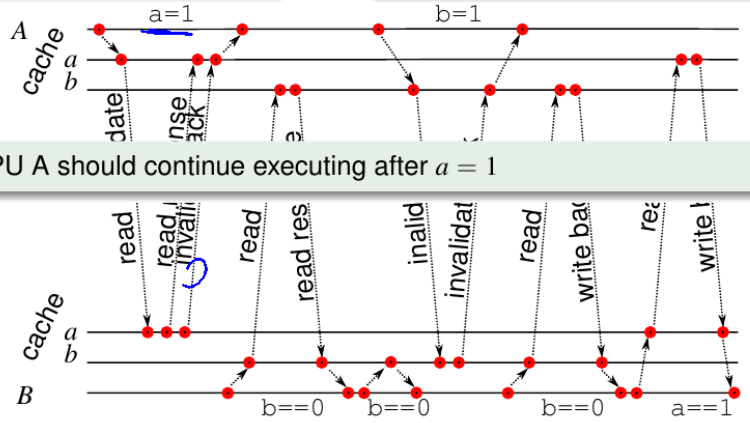

⇝ CPU A should continue executing after $a = 1$

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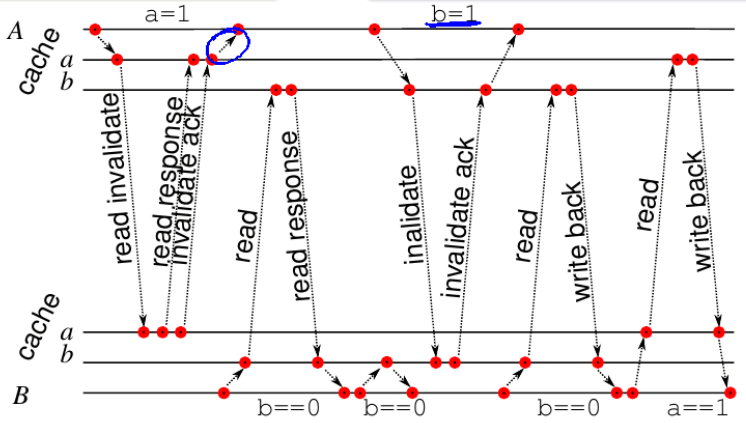
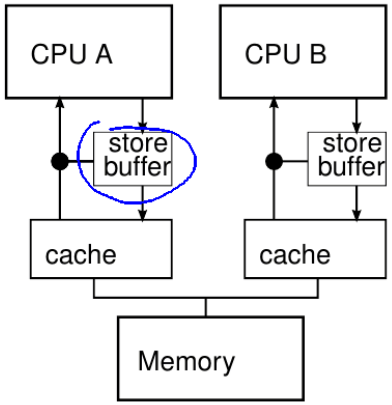


Store Buffers

Goal: continue execution after *cache-miss* write operation



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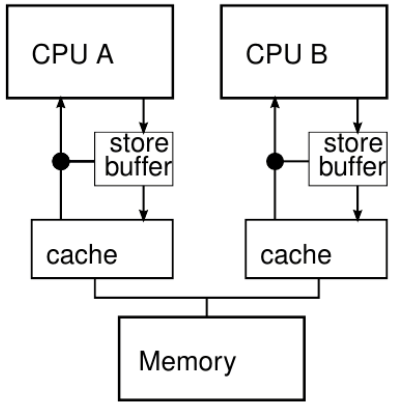

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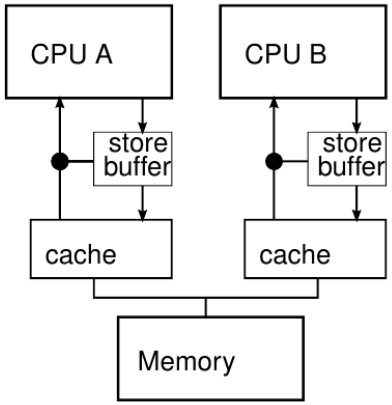

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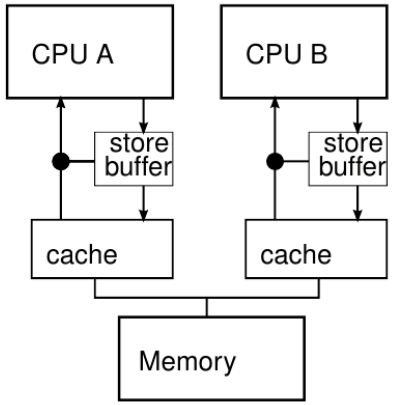

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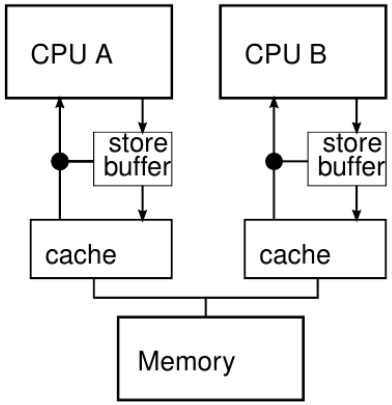

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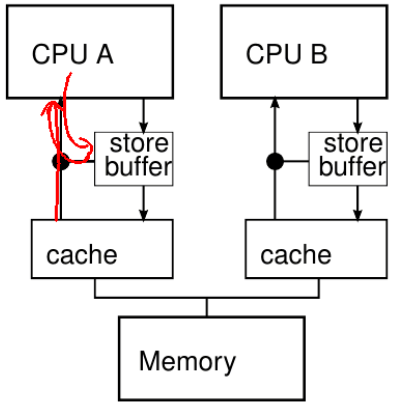

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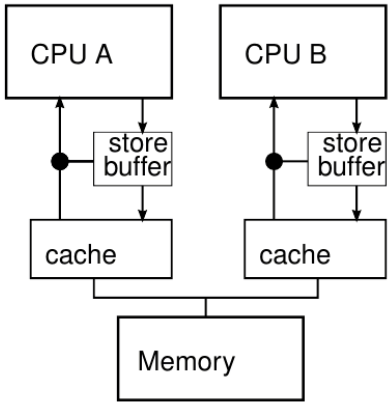

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  - on hit, return the youngest value that is waiting to be written

Happened-Before Model for Store Buffers

Thread A

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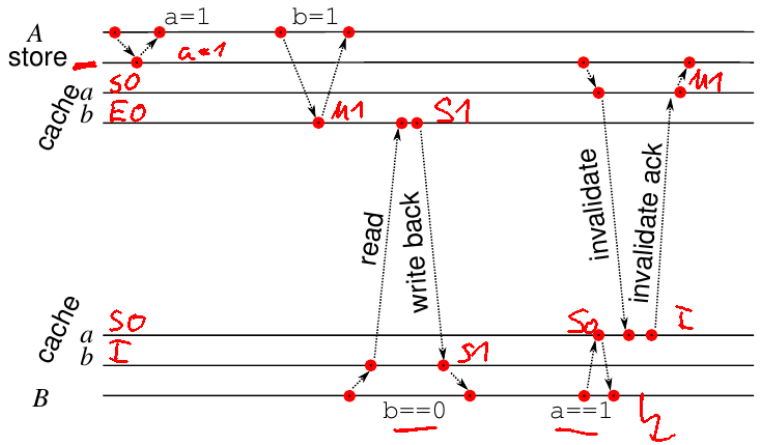
Assume cache A contains: a: S0, b: E0, cache B contains: a: S0, b: I



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Overtaking of messages *is desirable* and should not be prohibited in general.

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Memory Consistency | Out-of-Order Execution of Stores | 31 / 48

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assignment

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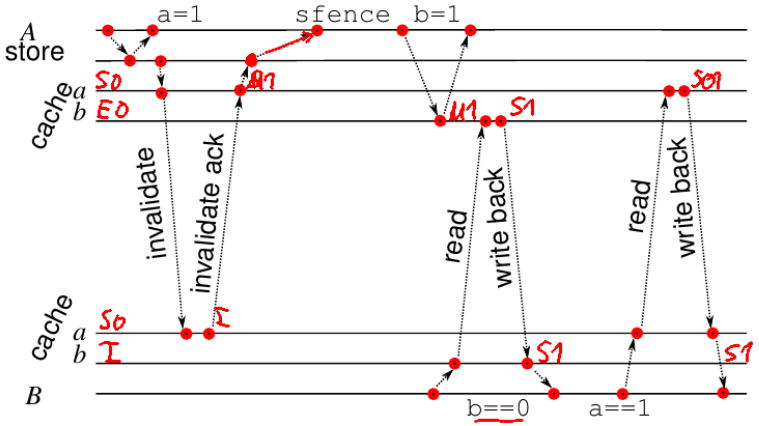

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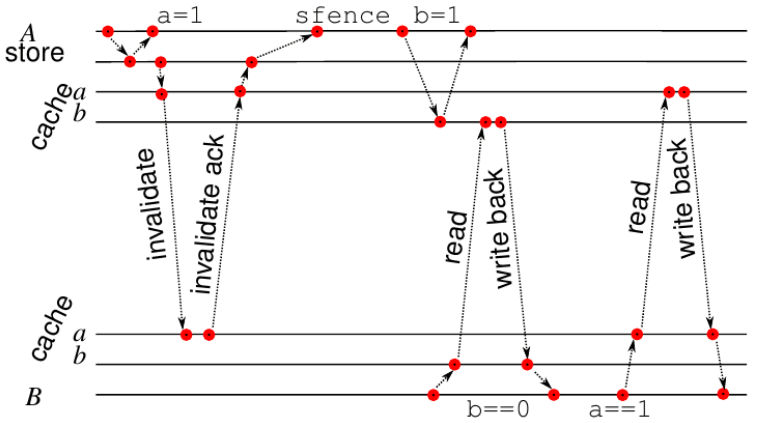

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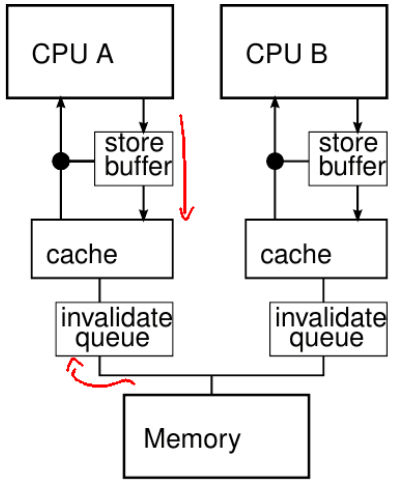

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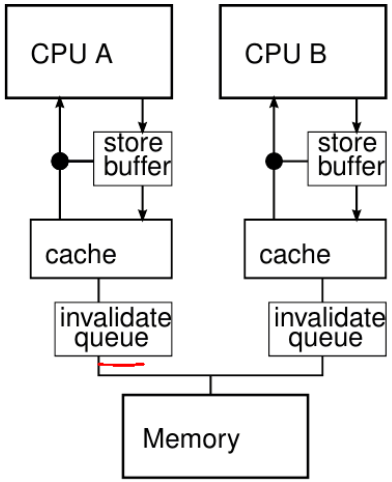

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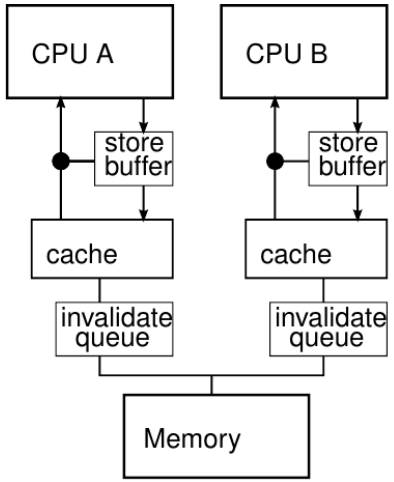

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- ⚠ local read and writes do *not* consult the invalidate queue

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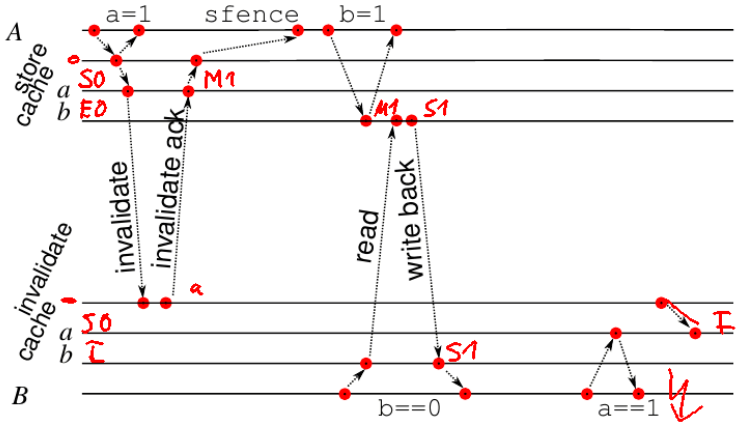

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$\rightsquigarrow$ match each write barrier in one process with a read barrier in another process

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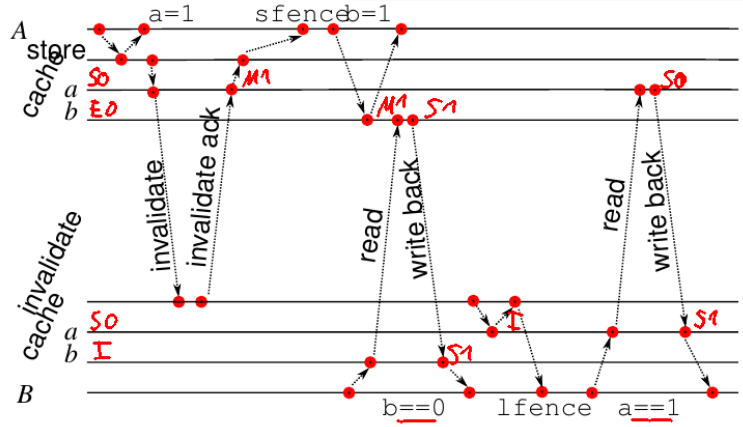

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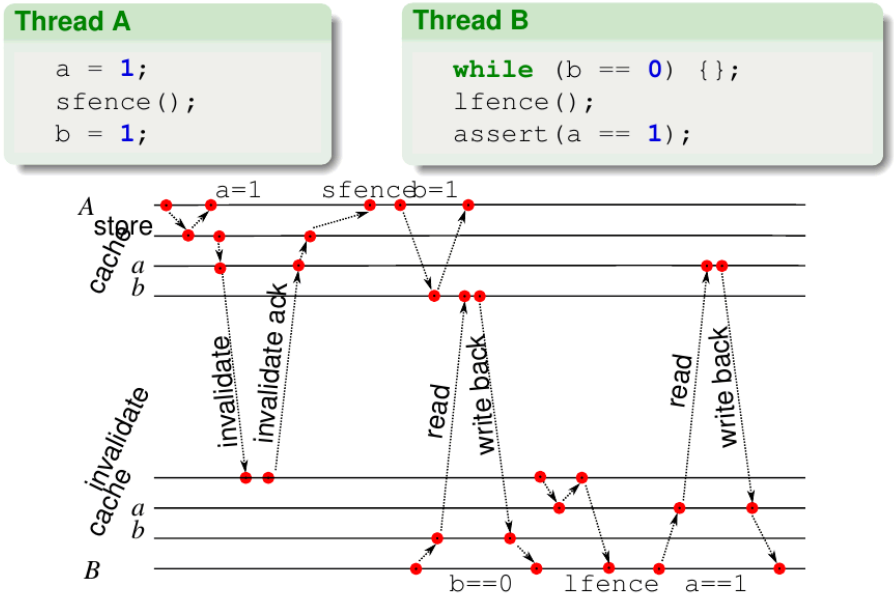

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- use the `volatile` keyword in C/C++
- in the latest C++ standard, an access to a `volatile` variable will automatically insert a memory barrier
- otherwise, inline assembler has to be used

⇝ memory barriers are the “lowest-level” of synchronization

Using Memory Barriers: the Dekker Algorithm

Mutual exclusion of two processes with busy waiting.

```
//flag[] is boolean array; and turn is an integer
flag[0] = false
flag[1] = false
turn    = 0   // or 1
```

```
P0:
flag[0] = true;
while (flag[1] == true)
  if (turn != 0) {
     flag[0] = false;
     while (turn != 0) {
       // busy wait
     }
     flag[0] = true;
  }
// critical section
turn    = 1;
flag[0] = false;
```

```
P1:
flag[1] = true;
while (flag[0] == true)
  if (turn != 1) {
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     while (turn != 1) {
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     flag[1] = true;
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turn    = 0;
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The Idea Behind Dekker

Communication via three variables:

- `flag[i]=true` process P_i wants to enter its critical section
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- if P_{1-i} also wants to enter, wait for `turn` to be set to `i`

The Idea Behind Dekker

Communication via three variables:

- `flag[i]=true` process P_i wants to enter its critical section
- `turn=i` process P_i has priority when both want to enter

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P0:
flag[0] = true;
while (flag[1] == true)
  if (turn != 0) {
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turn    = 1;
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In process P_i:

- if P_{1-i} does not want to enter, proceed immediately to the critical section
- $\rightsquigarrow$ `flag[i]` is a *lock* and may be implemented as such
- if P_{1-i} also wants to enter, wait for `turn` to be set to `i`
- while waiting for `turn`, reset `flag[i]` to enable P_{1-i} to progress
- algorithm only works for two processes

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- non-trivial program to parallelize
- idea: use two threads, one for `f` and one for `g`

Concurrent Reduce

Create an n-place buffer for communication between processes P_f and P_g.

```
T acc = init();
Buffer<U> buf = buffer<T>(n); // some locked buffer
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Pf:
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But busy waiting is bad!

- the cores might be idle anyway: no harm done (but: energy efficiency?)

Memory Consistency The Dekker Algorithm 41 / 48

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- *ideal scenario*: keep busy during busy waiting

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- general setup in signal/data processing
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Discussion

Memory barriers lie at the lowest level of synchronization primitives.
Where are they useful?

- when several processes implement an automaton and . . .

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What do compilers do about barriers?

- C/C++: it's up to the programmer, use `volatile` for all thread-common variables to avoid optimization that are only correct for sequential programs

Summary

Memory consistency models:

- strict consistency
- sequential consistency
- weak consistency

Illustrating consistency:

- happened-before relation
- happened-before process diagrams

Intricacy of cache coherence protocols:

- the effect of store buffers
- the effect of invalidate buffers
- the use of memory barriers

Use of barriers in synchronization algorithms:

- Dekker's algorithm
- stream processing, avoidance of busy waiting
- inserting fences

Future Many-Core Systems: NUMA

Symmetric multi-processing (SMP) has its limits:

- a memory-intensive computation may cause contention on the bus
- the speed of the bus is limited since the electrical signal has to travel to all participants
- point-to-point connections are faster than a bus, but do not provide possibility of forming consensus

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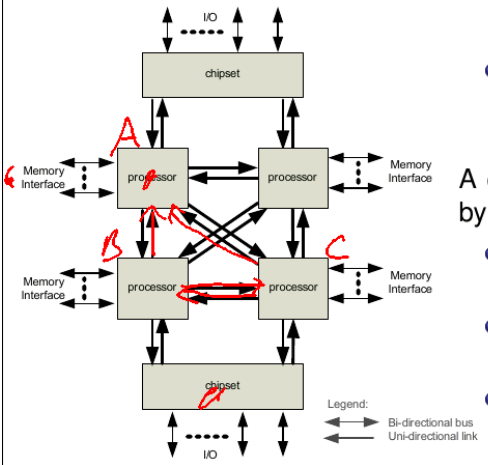
$\rightsquigarrow$ use a bus locally, use point-to-point links globally: NUMA

- non-uniform memory access *partitions* the memory amongst CPUs
- a directory states which CPU holds a memory region

Overhead of NUMA Systems

Communication overhead in a NUMA system.



source: [Int09]

- Processors in a NUMA system may be fully or partially connected.
- The directory of who stores an address is partitioned amongst processors.

A cache miss that cannot be satisfied by the local memory at A:

- A sends a retrieve request to processor B owning the directory
- B tells the processor C who holds the content
- C sends data (or status) to A and sends acknowledge to B
- B completes transmission by an acknowledge to A

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