Script generated by TTT

Title: Simon: Programmiersprachen (29.11.2013)

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Consistency During Transactions

Consistency during a transaction.

ACID states how committed transactions behave but not what may happen until a transaction commits.

- a transaction that is run on an inconsistent state may generate an inconsistent state ⇝ zombie transaction
- this is usually ok since it will be aborted eventually
- but transactions may cause havoc when run on inconsistent states

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atomic {                          // preserved invariant: x==y
  int tmp1 = x;                   atomic {
  int tmp2 = y;                     x = 10;
  assert(tmp1-tmp2==0);             y = 10;
}                                 }
```

- critical for C/C++ if, for instance, variables are pointers

Definition (opacity)

A TM system provides *opacity* if failing transactions are serializable w.r.t. committing transactions.

⇝ failing transactions still sees a consistent view of memory

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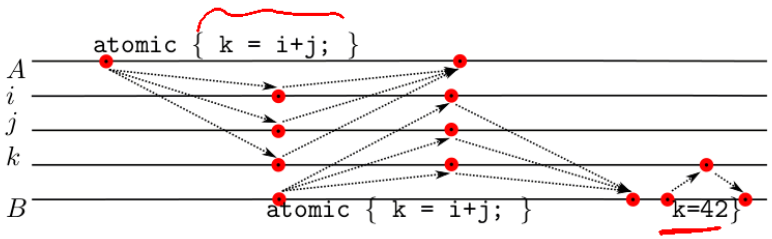
- *strong isolation*: retain order between accesses to TM and non-TM

Definition (SLA)

The *single-lock atomicity* is a model in which the program executes as if all transactions acquire a single, program-wide mutual exclusion lock.

⇝ like *sequential consistency*, SLA is a statement about program equivalence

Properties of Single-Lock Atomicity



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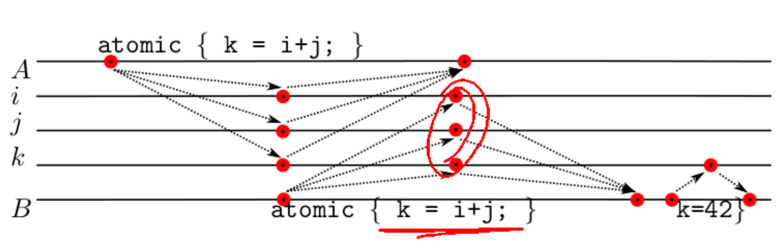

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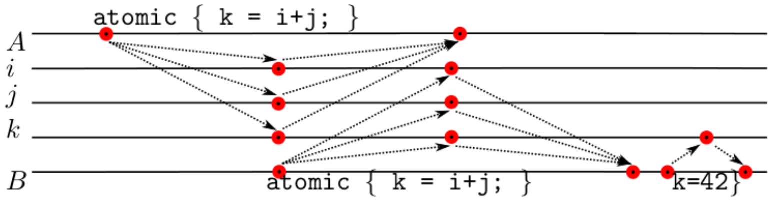

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- SLA enforces order between TM and non-TM accesses ✓
  - this guarantees *strong isolation* between TM and non-TM accesses
- within one transactions, accesses may be re-ordered ✓
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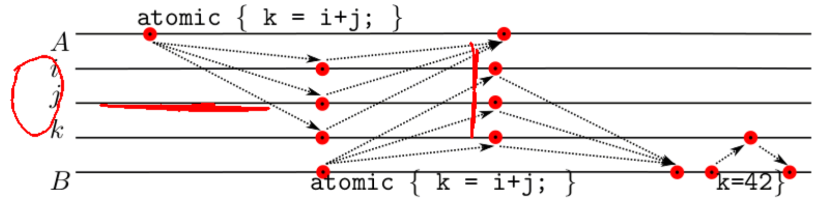

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- the content of non-TM memory conveys information which `atomic` block has executed, even if the TM regions do not access the same memory
  - SLA makes it possible to use `atomic` block for synchronization

Disadvantages of the SLA model

The SLA model is *simple* but often too strong:

1. SLA has a weaker *progress* guarantee than a transaction should have

```
// Thread 1
atomic {
  while (true) {};
}
```

```
// Thread 2
atomic {
  int tmp = x; // x in TM
}
```

2. SLA correctness is too strong in practice

```
// Thread 1
data = 1;
atomic {
}
ready = 1;
```

```
// Thread 2
atomic {
  int tmp = data;
  // Thread 1 not in atomic
  if (ready) {
    // use tmp
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- under the SLA model, `atomic {}` acts as barrier
- intuitively, the two transactions should be independent rather than synchronize

Transactional Sequential Consistency

How about a more permissive view of transaction semantics?

- TM should not have the blocking behaviour of locks
- ⇝ the programmer cannot rely on synchronization

Definition (TSC)

The *transactional sequential consistency* is a model in which the accesses within each transaction are sequentially consistent.

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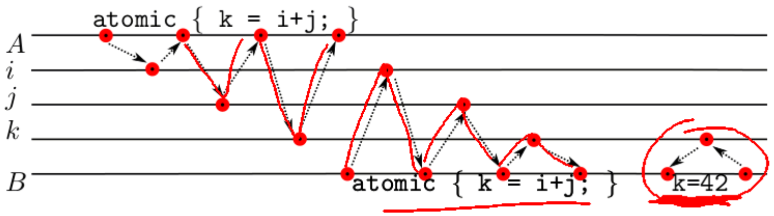

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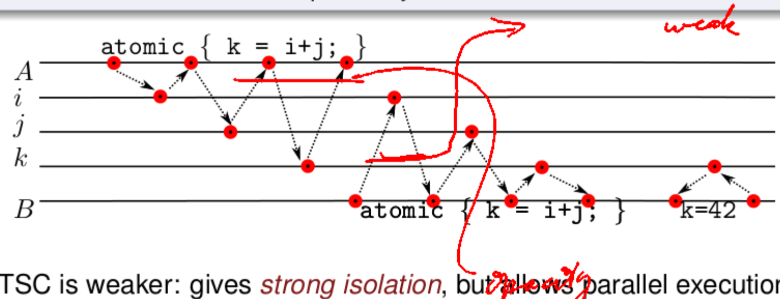

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⇝ actual implementations use TSC with some *race free* re-orderings

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atomic {                    do {
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- translation can be done using a pre-processor
  - determining a minimal set of memory accesses that need to be transactional requires a good static analysis
  - *idea*: translate all accesses to global variables and the heap as TM
  - more fine-grained control using manual translation
- an actual implementation might provide a `retry` keyword
  - when executing `retry`, the transaction aborts and re-starts
  - the transaction will again wind up at `retry` unless its *read set* changes
  - ⇝ block until a variable in the read-set has changed
  - similar to condition variables in monitors

Transactional Memory for the Queue

If a preprocessor is used, `PopRight` can be implemented as follows:

double-ended queue: removal

```
int PopRight(DQueue* q) {
  QNode* oldRightNode;
  atomic {
    QNode* rightSentinel = q->right;
    oldRightNode = rightSentinel->left;
    if (oldRightNode==leftSentinel) retry;
    QNode* newRightNode = oldRightNode->left;
    newRightNode->right = rightSentinel;
    rightSentinel->left = newRightNode;
  }
  int val = oldRightNode->val;
  free(oldRightNode);
  return val;
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- the transaction will abort if other threads call `PopRight`
- if the queue is empty, it may abort if `PushLeft` is executed

A Software TM Implementation

A software TM implementation allocates a *transaction descriptor* to store data specific to each `atomic` block, for instance:

- *undo-log* of writes if writes have to be undone if a commit fails
- *redo-log* of writes if writes are postponed until a commit
- *read-* and *write-set*: locations accessed so far
- *read-* and *write-version*: time stamp when value was accessed

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TL2 stores a *global version* counter and:

- a read version in each *object* (allocate a few bytes more in each call to `malloc`, or inherit from a *transaction object* in e.g. Java)
- a redo-log in the transaction descriptor
- a read- and a write-set in the transaction descriptor
- a read-version: the version when the transaction started

Principles of TL2

The idea: obtain a version `tx.RV` from the global clock when starting the transaction, the *read-version*, and set the versions of all written cells to a new version on commit.
A read from a field at `offset` of object `obj` is implemented as follows:

transactional read

```
int ReadTx(TMDesc tx, object obj, int offset) {
  if (&(obj[offset]) in tx.redoLog) {
    return tx.redoLog[&obj[offset]];
  } else {
    atomic { v1 = obj.timestamp; locked = obj.sem<1; };
    result = obj[offset];
    v2 = obj.timestamp;
    if (locked || v1 != v2 || v1 > tx.RV) AbortTx(tx);
  }
  tx.readSet = tx.readSet.add(obj);
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`WriteTx` is simpler: add or update the location in the redo-log.

Committing a Transaction

A transaction can succeed if none of the read locations has changed:

committing a transaction

```
bool CommitTx(TMDesc tx) {
  foreach (e in tx.writeSet)
    if (!try_wait(e.obj.sem)) goto Fail;
  WV = FetchAndAdd(&globalClock);
  foreach (e in tx.readSet)
    if (e.obj.version > tx.RV) goto Fail;
  foreach (e in tx.redoLog)
    e.obj[e.offset] = e.value;
  foreach (e in tx.writeSet) {
    e.obj = WV; signal(e.obj.sem);
  }
  return true;
Fail:
  // signal all acquired semaphores
  return false;
}
```


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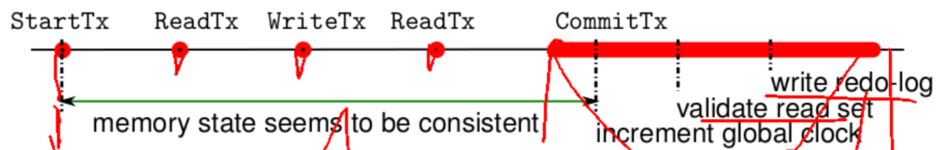

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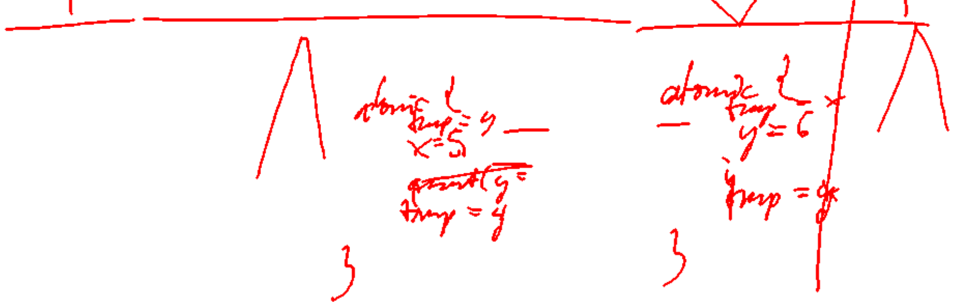

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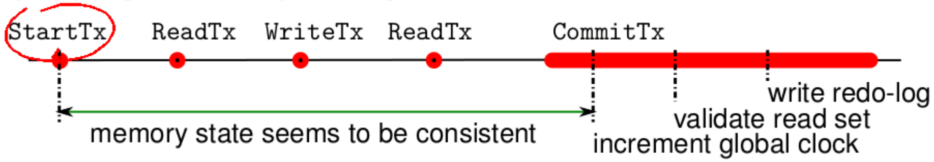

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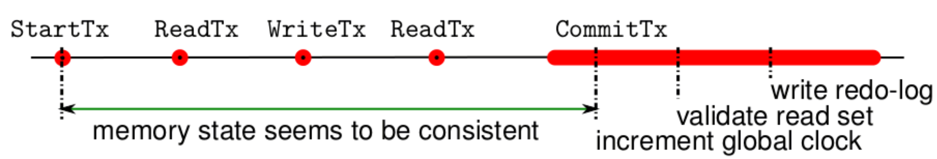

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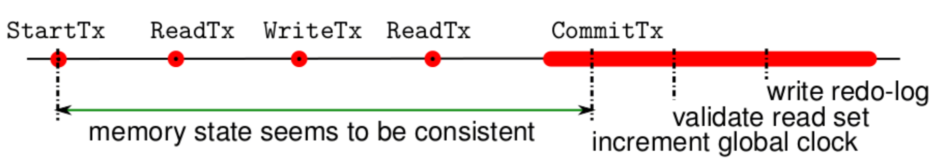

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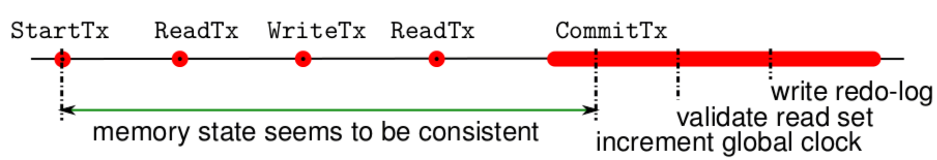

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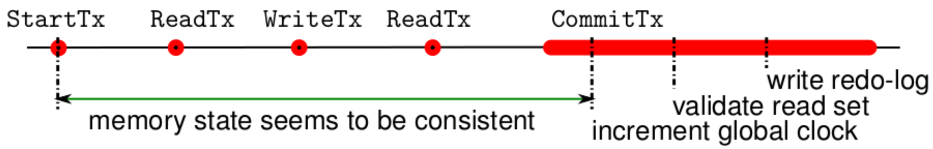

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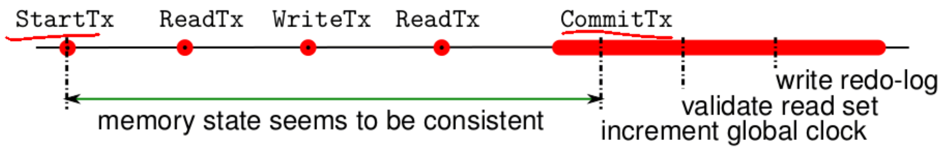

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  - read version+lock, `lfence`, read value, `lfence`, read version
- there might be contention on the global clock

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- lock-based commits can cause contention
  - organize cells that participate in a transaction in one object
  - compute a new object as result of a transaction
  - atomically replace a pointer to the old object with a pointer to the new object if the old object has not changed
  - ⇝ idea of the original STM proposal

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  - compute a new object as result of a transaction
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  - ⇝ idea of the original STM proposal
- TM system should figure out which memory locations must be logged

General Challenges when using TM

Executing `atomic` blocks by repeatedly trying to executing them non-atomically creates new problems:

- a transaction might unnecessarily be aborted
  - the granularity of what is locked might be too large
  - a TM implementation might impose restrictions:

```
// Thread 1                  // Thread 2
atomic {                     atomic {
  ...                          // x is shared
                               x = 42;
                             }
  int r = ReadTx(&x,0);
}
```

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- danger of live-locks: transaction B might abort A which might abort B . . .

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- *Prohibit It.* Certain constructs do not make sense. Use compiler to reject these programs.
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⇝ currently best to use TM only for memory; check if TM supports irrevocable transactions

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   - same instructions can be used, hardware interprets them as transactional

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Provides new instructions `XBEGIN`, `XEND`, `XABORT`, and `XTEST`:

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- `XBEGIN` takes an instruction address where execution continues if the transaction aborts
- `XEND` commits the transaction started by the last `XBEGIN`
- `XABORT` aborts the current transaction with an error code
- `XTEST` checks if the processor is executing transactionally

The instruction `XBEGIN` can be implemented as a C function:

```
int data[100]; // shared
void update(int idx, int value) {
  if(_xbegin()==-1) {
      data[idx] += value;
      _xend();
    } else {
      // transaction failed
    }
}
```

⇝ user must provide fall-back code

Considerations for the Fall-Back Path

Consider executing the following code in parallel with itself:

```
int data[100]; // shared
void update(int idx, int value) {
  if(_xbegin()==-1) {
      data[idx] += value;
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      data[idx] += value;
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Problem:

- if the fall-back code is executed, it might be interrupted by the transaction
- the write in the fall-back path thereby overwrites the value of the transaction

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⇝ need to ensure that the fall-back path is executed atomically

Protecting the Fall-Back Path

Use a lock to prevent the transaction from interrupting the fall-back path:

```
int data[100]; // shared
int mutex;
void update(int idx, int value) {
  if(_xbegin()==-1) {
      data[idx] += value;
      _xend();
    } else {
      wait(mutex);
      data[idx += value]
      signal(mutex);
    }
}
```

- fall-back path may not run in parallel with others ✓
- ⚠ transactional region may not run in parallel with fall-back path

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Transactional operation:

- augment each cache line with an extra bit T

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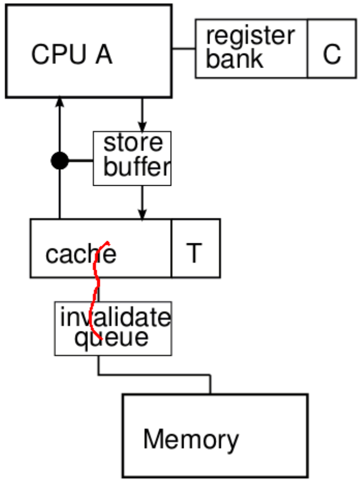

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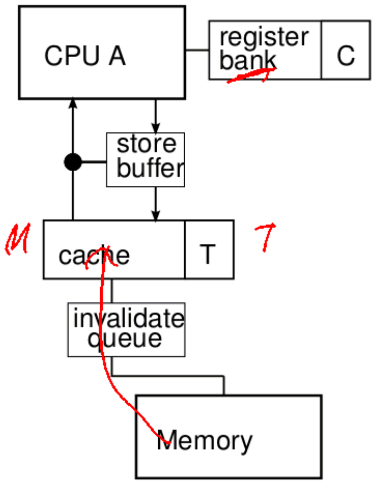

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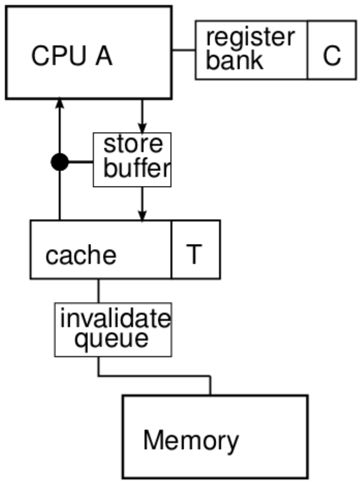

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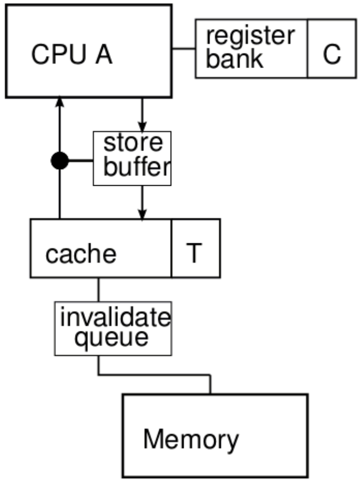

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- `XABORT` clears all T flags, sets $C = 0$ and restores CPU registers
- `XCOMMIT` decrement C and, if $C = 0$, clear all T flags

Illustrating Transactions

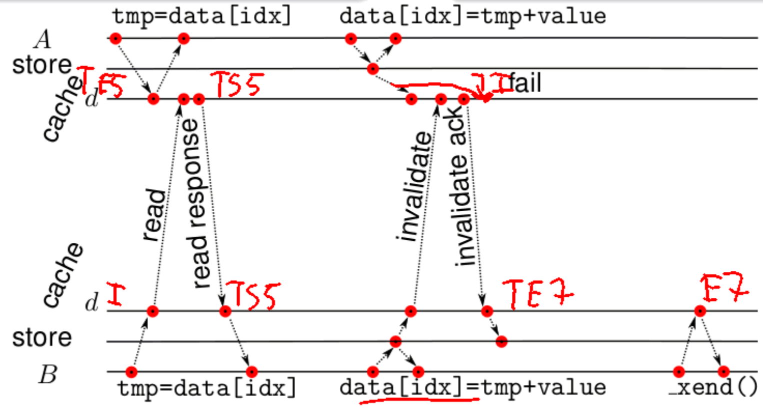
Augment MESI state with extra bit T per cache line. CPU A: E5, CPU B: I

Thread A

```
int tmp = data[idx];
data[idx] = tmp+value;
_xend();
```

Thread B

```
int tmp = data[idx];
data[idx] = tmp+value;
_xend();
```



Common Code Pattern for Mutexes

Using HTM in order to implement mutex:

```
int data[100]; // shared
int mutex;
void update(int idx, int value) {
  if(_xbegin()==-1) {
    if (mutex>0) _xabort();
    data[idx] += value;
    _xend();
  } else {
    wait(mutex);
    data[idx += value]
    signal(mutex);
  }
}
```

```
void update(int idx, int val) {
  lock(mutex);
  data[idx] += val;
  unlock(mutex);
}
void lock(int mutex) {
  if(_xbegin()==-1)
    if (mutex>0) _xabort();
    else return;
  wait(mutex);
}
void unlock(int mutex) {
    if (mutex>0) signal(mutex);
    else _xend();
}
```

- the critical section may be executed with an *elided* lock
- as soon as one thread conflicts, the mutex will be taken, thereby aborting all other transactions that have read `mutex`

Hardware Lock Elision

Observation: Using HTM to implement lock elision is a common pattern
⇝ provide special handling in hardware: HLE

- provides a way to execute a critical section without the overhead of the atomic updates necessary to acquire and release the lock

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- all but one elided lock may abort ⇝
  - progress guarantee since lock is taken on abort
  - no back up path is required

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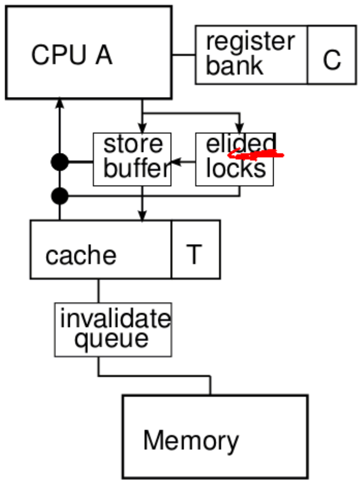
Transactional operation:

- re-uses infrastructure for Restricted Transactional Memory
- add a buffer for elided locks, similar to store buffer



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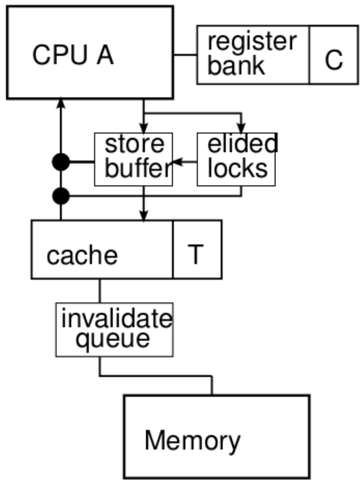

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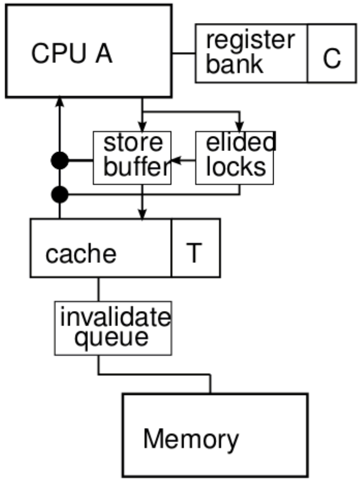

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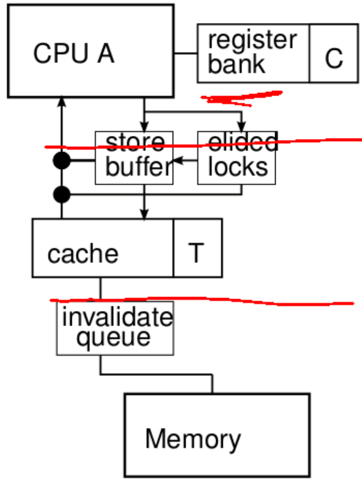

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- if irrevocable, clear all T flags, set $C = 0$ and move elided buffer to store buffer

References

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